Amendments to the Specification:

Please replace paragraph [13] on page 3 of the specification with the following amended paragraph:

[13] The system clock 12 is typically operative to produce a square wave output at 13 MHz. The preferred master clock frequency is 39 MHz, which has as factors 1300 and 95. Accordingly, a programmable reference divider 16 is coupled to receive the master clock frequency signal. The programmable divider 16 is a subsystem which produces output square wave signals which are selective designated by [[by]] means of a channel spacing selector 18 or equivalent, which is operative to instruct the divider 16 to operate with a divisor of either the first integer value of 1300 or at the second integer value of 95 to produce respectively the first channel spacing clock signal of 30 kHz and the second channel spacing clock signal at 200 kHz.

Please replace paragraph [14] on page 3 of the specification with the following amended paragraph:

[14] A frequency synthesizer as hereinafter explained is controlled by these two clock signals. The synthesizer has a digital phase detector 20 coupled to receive output of the programmable reference divider 16 to detect the phase of both the first channel spacing clock signal and the second channel spacing clock signal. The digital phase detector 20 receives as a reference input a digital feedback signal to which it can lock. The digital phase detector 20 produces as output an analog phase error signal in the form of a

steering voltage after being filtered by a lowpass filter 22. The steering voltage is input to a voltage controlled oscillator (VCO) 24 which serves as the phase error signal. The VCO 24 serves as a band selector RF source which generates a frequency controlled analog radio frequency (RF) signal at one or the other of the desired frequency for system output, namely 840 MHz or 1900 MHz. These signals are fed to the amplifier stage of the host system. These signals are also fed into the feedback signal path where a limiting amplifier 26 yields amplitude-limited clock signals of the respective frequencies 840 MHz and 1900 MHz.

Please replace the originally-filed Abstract of the disclosure with the Abstract of the disclosure attached to the end of this Preliminary Amendment.